REMARKS/ARGUMENTS

Claims 1-14, 18 and 20-31 are pending in this application. Claims 18 and 20-23 are allowed. Claims 1-3, 5-10, 12-14 and 24-31 are rejected. Claims 4 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims. Claims 1, 2, 8, 9, and 28 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,449,701 to Cho and U.S. Patent No. 6,272,600 to Talbot et al. Claims 3, 5-7, 10, 12-14, 29, 30, and 31 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,449,701 to Cho and U.S. Patent No. 6,272,600 to Talbot et al and U.S. Patent No. 5,802,571 to Konigsburg et al. Claim 24 is rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,272,600 to Talbot et al. Claims 25, 26, and 27 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,272,600 to Talbot et al. and U.S. Patent No. 5,802,571 to Konigsburg et al. Claim 25 is cancelled. Claim 24 is amended. Applicants gratefully acknowledge the Office Action's indication that claim 18 and 20-23 are allowable and claims 4 and 11 contain allowable subject matter.

Applicants respectfully submit the cited reference do not teach suggest or disclose "[a] graphics device comprising: ... a multipurpose buffer mechanism to simultaneously monitor a status of said plurality of data requests ..." (as described in the embodiment of claim 1.

The Office Action asserts that Cho teaches these features in columns 4-10, and figure 2 and more specifically that compare circuitry in request queue 40 sets an issued

indication (Iss) to a state indicating that the transaction has been issued. Column 8 lines 4-13 state:

> Compare circuitry in request queue 40 *may compare the data buffer pointers (Ptr) returned* by channel control circuit 42A *to the data buffer pointers in each queue entry to identify which transaction is being acknowledged*, and an issued indication (Iss in each queue entry illustrated in FIG. 2) may be set to a state indicating that the transaction has been issued. The transaction may not be considered for subsequent issuance by control circuit 50 when the issued indication is in a state indicating that the transaction has been issued. For example, the issued indication may be a bit. *(emphasis added)*

Applicants submit Cho teaches a control circuit for the request queue may issue addresses from the request queue to the channel control circuit out of order, and thus the memory operations may be completed out of order. The above section discloses monitoring of the data buffer pointers (Ptr) returned by channel control circuit 42A and fails to disclose a multipurpose buffer mechanism to simultaneously monitoring a status of a plurality of data requests. It is noted that by identifying which transaction is being acknowledged, the compare circuitry of Cho is not monitoring the status of a data request in the buffer (as specifically recited in the embodiment of independent claim 1), rather, it is monitoring activities occurring outside of the buffer, namely in the memory.

However, the Office Action does not cite to a section in Cho that discloses the limitations detailed above, but rather merely asserts Cho discloses monitoring the status of data requests generally. This is inadequate to form the basis of a proper §103(a) rejection.

Talbot fails to cure the deficiencies of Cho. Talbot relates to a system that carries out memory transactions in an order that maximizes concurrency in a memory system such as a multi-bank interleaved memory system. Read data is collected in a buffer

memory to be presented back to the bus in the same order as read transactions were requested, even though requests had been presented to the memory system in a different order. Talbot is devoid of any teaching or suggestion of "simultaneously monitor[ing] a status of said plurality of data requests" as specifically recited in the embodiment of claim 1.

Lastly, Applicants submit the rejection of independent claim 8 on the same grounds as independent claim 1 is improper and that the cited references do not teach "[a] system to process a plurality of data requests, said system comprising: ... a multipurpose buffer mechanism *to maintain an ordering of said data requests* to said plurality of memory locations and data responses from said plurality of memory locations (e.g. as described in the embodiment of claim 8). Clearly, at the least *maintaining an ordering of data requests* different than *monitoring a status of data request.* Therefore, the rejection of independent claim 8 based on the 35 U.S.C. 103(a) rejection of claim 1 is improper, and a proper rejection including each and every limitation of independent claim 8 must be forwarded. Moreover, Applicants note that independent claim 8 contains similar limitations to that found in previously allowed independent claim 20, and thereby submit that claim 8 is in allowable form as well.

Therefore, since each and every element of claim 1 is not taught, suggested or disclosed by the cited reference, Applicant respectfully submits that the 103(a) rejections are lacking and should be withdrawn. Likewise claims 24 and 28 include similar limitations. Claims 2-7, 9-14, 18, 25-27, and 29-31 depend from and further define allowable independent claims 1, 8, 24, and 28 and therefore are allowable as well.

For at least all the above reasons, the Applicants respectfully submit that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. § 1.16 or § 1.17 to Deposit Account No. **11-0600**.

Respectfully submitted,

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